UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,380	06/30/2003	Roni Rosner	42P17037	1513

8791 7590 03/07/2007

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/611,380	ROSNER ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 are pending.

Papers Filed

2. Examiner acknowledges receipt of remarks and amended claims, filed on 31 October 2006 and RCE filed on 05 December 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Strombergson et al. (U.S. Patent No. 6,807,621) hereinafter referred to as Strombergson.

5. As per claim 1, Strombergson discloses a device comprising:

a first device (Fig. 1 reservation unit 3A in combination with execution unit 4A) to track segment order associated with a first execution unit (Fig. 1 execution unit 4A);

a second device (Fig. 1 reservation unit 3B in combination with execution unit 4B) to track segment order associated with a second execution unit (Fig. 1 execution

unit 4B); *The examiner asserts that a single instruction constitutes a segment of the program running on Strombergson's processor. Further, the examiner asserts that the reservation unit 3A/B receives instructions intended for execution unit 4A/B. The reservation unit tracks instructions. Col. 4 lines 45-51 dictate that instructions are checked for irregularities in the order that they were received at the decode stage. The reservation unit must inherently track instruction order if it is to check for irregularities in the proper order.*

and a third device (Fig. 1 commit stage 5) coupled to the first device and second device to track relative segment order between the first device and the second device. *The examiner asserts that the commit stage is coupled to the first and second execution and reservation units as pictured in Fig. 1. Further, the reorder buffer must track instructions through all execution units. If the reorder buffer did not keep track of instruction order, instructions would not be guaranteed to complete in the proper order, causing undesired operation of the processor.*

6. As per claim 2, Strombergson discloses the device of claim 1, wherein the first device (Fig. 1 reservation unit 3A in combination with execution unit 4A) is operable to notify the third device (Fig. 1 commit stage 5) of a mispredicted instruction in a segment, and wherein the first device is operable to flush a first segment. (Col. 3 lines 34-60)

7. As per claim 3, Strombergson discloses the device of claim 2, wherein the third device (Fig. 1 commit stage 5) is operable to notify the second device (Fig. 1

reservation unit 3B in combination with execution unit 4B) of the mispredicted instruction in the segment, and wherein the second device is operable to flush a second segment. (Col. 3 lines 34-60)

8. As per claim 4, Strombergson discloses the device of claim 2, wherein the third device (Fig. 1 commit stage 5) is operable to notify the first device (Fig. 1 reservation unit 3A in combination with execution unit 4A) of the mispredicted instruction in the segment, and wherein the first device is operable to flush a third segment. (Col. 3 lines 34-60)

As per claim 5, Strombergson discloses the device of claim 1, further comprising: a fetch control unit (Fig. 1 fetch unit 1 in combination with decode unit 2) to predict segment order (Col. 4 line 57-58), fetch segments and assign the segments to one of the first device and the second device during a flush operation. (Col. 7 lines 42-54)

1. As per claim 6, Strombergson discloses a method comprising:

tracking the program order of a first set of instructions assigned to a first local reorder buffer (Fig. 1 reservation unit 3A in combination with execution unit 4A) in a first execution unit (Fig. 1 reservation unit 3A in combination with execution unit 4A);

tracking the program order of a second set of instructions assigned to a second local reorder buffer (Fig. 1 reservation unit 3B in combination with

execution unit 4B) in a second execution [unit] (Fig. 1 reservation unit 3B in combination with execution unit 4B);

and tracking program order of the first set of instructions relative to the second set of instructions in a global reorder buffer (Fig. 1 commit stage 5). *The examiner asserts that since the commit stage contains a reorder buffer (ROB 10), the stage is responsible to for tracking program order from all the execution stages.*

9. As per claim 7, Strombergson discloses the method of claim 6, further comprising:

notifying the global reorder buffer (Fig. 1 commit stage 5) when a mispredicted instruction occurs; (Col. 3 lines 34-60)

intiating a flush operation in the global reorder buffer (Fig. 1 commit stage 5); (Col. 3 lines 34-60)

and notifying the first local reorder buffer (Fig. 1 reservation unit 3A in combination with execution unit 4A) of the mispredicted instruction. (Col. 3, lines 34-60)

10. As per claim 8, Strombergson discloses the method of claim 7, further comprising: notifying a fetch control unit (Fig. 1 fetch unit 1 in combination with decode unit 2) of a mispredicted set of instructions. (Col. 3 line 51)

11. As per claim 9, Strombergson discloses the method of claim 6, further comprising: sending a signal to the second local reorder buffer (Fig. 1 reservation unit 3B in combination with execution unit 4B) to flush at least a third set of instructions. (Col. 3 line 58-60)

12. As per claim 10, Strombergson discloses the method of claim 6, further comprising: fetching a fourth set of instructions; and assigning the fourth set of instruction to the first reorder buffer during a flushing operation. *The examiner asserts that the processor will continue to process instructions, starting with the branch target instruction, after a conditional branch has been taken. These instructions will be issued to the functional stages, including the stage including the first reorder buffer, and will be executed once the flushing of the stage has been completed.*

13. As per claim 11, Strombergson discloses the method of claim 6, further comprising: retiring an instruction according to an indicator stored in the global reorder buffer(Fig. 1 commit stage 5). (Col. 8 lines 22-27) *The examiner asserts that indicators must exist to reorder instructions after execution.*

14. As per claim 12, Strombergson discloses a system comprising:

a bus; (Fig. 1, line connecting memory 7 to fetch unit 1)

a memory device coupled to the bus; (Fig. 1 memory 7)

and a processor including a fetch control unit (Fig. 1 fetch unit 1 and decode unit 2) to fetch instructions from the memory device, a first execution unit (Fig. 1 reservation unit 3A in combination with execution unit 4A) to process one or more of the fetched instructions, a second execution unit (Fig. 1 reservation unit 3B in combination with execution unit 4B) to process one of more of the fetched instructions, a first reorder buffer (Fig. 1 reservation unit 3A in combination with execution unit 4A) to track instructions assigned to the first execution unit, a second reorder buffer (Fig. 1 reservation unit 3B in combination with execution unit 4B) to track instructions assigned to the second execution unit, and a global reorder buffer (Fig. 1 commit stage 5) to track instruction order of instructions assigned to the first reorder buffer relative to the second reorder buffer. (Col. 8 lines 22-27) *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed. The examiner asserts that the reorder buffer 10 in commit stage 5 tracks the order of instructions as it retires instructions in their proper order.*

15. As per claim 13, Strombergson discloses the system of claim 12, wherein the first reorder buffer is operable to signal the global reorder buffer upon detection of a mispredicted instruction. (Col. 3 lines 34-60)

16. As per claim 14, Strombergson discloses the system of claim 12, wherein the first reorder buffer is operable to flush a first set of instructions upon detection of a mispredicted instruction (Col. 3 lines 34-60), and wherein the fetch control unit assigns a second set of instructions to the first reorder buffer based on a set of load balancing criteria. *The examiner asserts that the processor will continue to process instructions, starting with the branch target instruction, after a conditional branch has been taken. These instructions will be issued to the functional stages, including the stage including the first reorder buffer, and will be executed once the flushing of the stage has been completed.*

17. As per claim 15, Strombergson discloses a machine readable medium having stored therein instructions, which when executed cause a machine to perform a set of operations comprising:

tracking the program order of a first set of instructions assigned to a first local tracking device in a first execution unit (Fig. 1 reservation unit 3A in combination with execution unit 4A); *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed.*

tracking the program order of a second set of instructions assigned to a second local tracking device in a second execution unit (Fig. 1 reservation unit 3B in combination with execution unit 4B); *The examiner asserts that the*

reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed.

and tracking program order of the first set of instructions relative to the second set of instructions in a global tracking device. (Fig. 1 commit stage 5) *The examiner asserts that the reorder buffer 10 in commit stage 5 tracks the order of instructions as it retires instructions in their proper order.*

18. As per claim 16, Strombergson discloses the machine readable medium of claim 15, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising: notifying the global tracking device (Fig. 1 commit stage 5) when a mispredicted instruction occurs. (Col. 3 line 55-57)

19. As per claim 17, Strombergson discloses the machine readable medium of claim 16, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising: tracking a first set of switch points in the global tracking device (Fig. 1 commit stage 5). *The examiner further asserts that the reorder buffer 10 tracks a given instruction compared to prior and subsequent instructions to maintain proper instruction ordering.*

20. As per claim 18, Strombergson discloses the machine readable medium of claim 16, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising: flushing a second set of switch points

based on the mispredicted instruction. *The examiner asserts that when a conditional branch instruction is mispredicted, instructions currently in other stages of the pipeline are flushed as described in col. 3 lines 34-60.*

21. As per claim 19, Strombergson discloses an apparatus comprising:

a means for tracking the program order of a first set of instructions assigned to a first local tracking device (Fig. 1 reservation unit 3A in combination with execution unit 4A) in a first execution unit (Fig. 1 reservation unit 3A in combination with execution unit 4A); *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed.*

a means for tracking the program order of a second set of instructions assigned to a second local tracking device (Fig. 1 reservation unit 3B in combination with execution unit 4B) in a second execution unit (Fig. 1 reservation unit 3B in combination with execution unit 4B); *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed.*

and a means for tracking program order of the first set of instructions relative to the second set of instructions in a global tracking device. (Fig. 1 commit stage 5) *The examiner asserts that the reorder buffer 10 in commit stage 5 tracks the order of instructions as it retires instructions in their proper order.*

22. As per claim 20, Strombergson discloses the apparatus of claim 19, further comprising: a means for notifying the global tracking device when a mispredicted instruction occurs. (Col. 3 lines 34-60)

23. As per claim 21, Strombergson discloses the apparatus of claim 19, further comprising: a means for flushing at least a third set of instructions in the first local tracking device. (Col. 3 lines 34-60)

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strombergson.

Regarding claims 22-26, Strombergson discloses the method and apparatus of claims 1, 6, 12, 15 and 19, comprising data for a set of switch points (col 1 lines 26-30).

Strombergson discloses in col 1 lines 26-30 that "super-scalar processors are also known which comprise multiple pipelines processing instructions simultaneously when adjacent instructions have no data dependencies between them." It follows then, in many processing systems, that these instructions that were intended for a particular

execution unit, are transitioned to another execution unit once their data dependencies are evaluated just prior to execution. Strombergson, however, does not particularly disclose this strategy.

Examiner takes Official Notice that it is common in the art to transition an instruction intended for a particular execution unit to a different execution unit as the data dependencies are evaluated.

Strombergson would have been motivated to utilize this technique in order to maximize instruction level parallelism making the processing system more efficient in order to optimize the technique described in col 1 lines 26-30.

Each of the new claims discloses "data for a set of switch points". Applicant's specification states that, "A switch point is the first segment in a sequence of consecutive segments that have been assigned to a single execution cluster or local order buffer." This appears to be an adequate definition that can be properly read into the claims. The "segments", however, are shown in some embodiments to be sequences of instructions, but do not have an appropriate definition that can be read into the claims. Segments will be interpreted to be a plurality of instruction bits. This may include a portion of an instruction, an entire instruction, or several instructions. It then follows that the "switch points" are also instruction bits. The claims, in particular, each state that the data for the switch points indicate a transition in consecutive segment (instruction assignment) from the first execution unit to the second execution unit. In essence, it appears that claim requires that instruction data override some pre-

existing or default decision to go to a particular execution unit and, in part, assign one or more instructions to a different execution unit.

Therefore, it would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Strombergson and allow the data for a set of switch points (data operand values for one or more instructions), the data indicating (by data dependencies) a transition in assignment of consecutive sets of instructions (in cases of multiple dependencies) from the first execution unit to the second execution unit (to improve instruction level parallelism).

Response to Arguments

4. Applicant's arguments filed 31 October 2006 have been fully considered but they are not persuasive.

5. The arguments presented appear all to be based on a single issue that was addressed in the advisory action mailed on 21 November 2006. The relevant statement is presented below for Applicant's convenience:

> *"Applicant states that...'the commit stage is keeping track of the overall program (or absolute order) via the reorder buffer, while the commite stage does not track program order of the first set of instructions relative to the second set of instructions.' Examiner disagrees. If an absolute order is tracked, then a relative order must be tracked. If the processor knows the exact position of each*

instruction, the processor knows the position of each instruction relative to the position of another instruction."

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100